What is claimed is:

1. A semiconductor wafer comprising:

a semiconductor body which includes an integrated circuit, an interconnect which is electrically connected with the integrated circuit, and a pad which is an end portion of the interconnect and is formed on a surface of the semiconductor body;

a redistribution layer which is formed over the semiconductor body, is electrically connected with the pad, and includes a first portion located over the pad and a second section other than the first portion;

a first resin layer which is formed over the redistribution layer;

a second resin layer which is formed over the first resin layer and covers a side surface of the first resin layer; and

an external terminal which is formed over the second section of the redistribution layer and is electrically connected with the redistribution layer.

2. The semiconductor wafer as defined in claim 1,

wherein the first resin layer is formed to cover the redistribution layer excluding a region in which the external terminal is formed, and

wherein the second resin layer is formed to cover at least a lower part of the external terminal.

3. The semiconductor wafer as defined in claim 1, further comprising an insulating layer under the redistribution layer.

4. The semiconductor wafer as defined in claim 1,

wherein the semiconductor wafer includes a first region and a plurality of second regions, each of the second regions being surrounded by the first region, and

wherein the first resin layer and the second resin layer are formed only in the second region.

5. The semiconductor wafer as defined in claim 4,

wherein a part of the second resin layer which covers the side surface of the first resin layer is formed in a upper part and along an edge portion of the second region.

6. A semiconductor device comprising:

a semiconductor body which includes an integrated circuit, an interconnect which is electrically connected with the integrated circuit, and a pad which is an end portion of the interconnect and is formed on a surface of the semiconductor body;

a redistribution layer which is formed over the semiconductor body, is electrically connected with the pad, and includes a first portion located over the pad and a second section other than the first portion;

a first resin layer which is formed over the redistribution layer;

a second resin layer which is formed over the first resin layer and covers a side surface of the first resin layer; and

an external terminal which is formed over the second section of the redistribution layer and is electrically connected with the redistribution layer.

7. The semiconductor device as defined in claim 6,

wherein the first resin layer is formed to cover the redistribution layer excluding a region in which the external terminal is formed, and

wherein the second resin layer is formed to cover at least a lower part of the external terminal.

8. The semiconductor device as defined in claim 6, further comprising an

insulating layer under the redistribution layer.

9. A circuit board on which the semiconductor device as defined in claim 6 is mounted.

10. Electronic equipment comprising the semiconductor device as defined in claim 6.

11. A method of manufacturing a semiconductor device comprising:

forming a redistribution layer over a semiconductor wafer which includes an integrated circuit and an interconnect electrically connected with the integrated circuit, the redistribution layer electrically connecting with a pad which is a part of the interconnect and including a first portion located over the pad and a second section other than the first portion;

forming an external terminal on the second section of the redistribution layer;

forming a first resin layer having a side surface so that at least a part of the first resin layer is placed on the redistribution layer;

forming a second resin layer over the first resin layer so as to cover the side surface of the first resin layer; and

cutting the semiconductor wafer.

12. The method of manufacturing a semiconductor device as defined in claim 11, comprising:

forming the first resin layer to cover the redistribution layer excluding a region in which the external terminal is formed, and

forming the second resin layer to cover at least a lower part of the external terminal.

13. The method of manufacturing a semiconductor device as defined in claim 11, further comprising:

forming an insulating layer before forming the redistribution layer,

wherein the redistribution layer is formed on the insulating layer.

14. The method of manufacturing a semiconductor device as defined in claim 11,

wherein the semiconductor wafer includes a first region and a plurality of second regions, each of the second regions being surrounded by the first region,

wherein the first resin layer and the second resin layer are formed only in the second region, and

wherein the semiconductor wafer is cut along the first region.

15. The method of manufacturing a semiconductor device as defined in claim 12,

wherein the semiconductor wafer includes a first region and a plurality of second regions, each of the second regions being surrounded by the first region,

wherein the first resin layer and the second resin layer are formed only in the second region, and

wherein the semiconductor wafer is cut along the first region.

16. The method of manufacturing a semiconductor device as defined in claim 13,

wherein the semiconductor wafer includes a first region and a plurality of second regions, each of the second regions being surrounded by the first region,

wherein the first resin layer and the second resin layer are formed only in the second region, and

wherein the semiconductor wafer is cut along the first region.

17. The method of manufacturing a semiconductor device as defined in claim 11, comprising:

forming a part of the second resin layer which covers the side surface of the first resin layer, in a upper part and along an edge portion of the second region.

18. The method of manufacturing a semiconductor device as defined in claim 11, wherein the second resin layer is formed by using a resin that is sensitive to radiation and by applying lithographic technology.

19. The method of manufacturing a semiconductor device as defined in claim 11, wherein the second resin layer is formed by ejecting a resin by using an ink-jet method.

20. The method of manufacturing a semiconductor device as defined in claim 11, wherein the second resin layer is formed by applying a resin by using a printing method.

21. A semiconductor wafer comprising:

a semiconductor body which includes an integrated circuit, an interconnect which is electrically connected with the integrated circuit, and a pad which is an end portion of the interconnect and is formed on a surface of the semiconductor body;

a wiring pattern which is formed over the semiconductor body, is electrically connected with the pad, and includes a first portion located over the pad and a second section other than the first portion;

a first resin layer which is formed over the wiring pattern;

a second resin layer which is formed over the first resin layer and covers a side surface of the first resin layer; and

an external terminal which is formed over the second section of the wiring pattern and is electrically connected with the wiring pattern.

22. A semiconductor device comprising:

a semiconductor body which includes an integrated circuit, an interconnect which is electrically connected with the integrated circuit, and a pad which is an end portion of the interconnect and is formed on a surface of the semiconductor body;

a wiring pattern which is formed over the semiconductor body, is electrically connected with the pad, and includes a first portion located over the pad and a second section other than the first portion;

a first resin layer which is formed over the wiring pattern;

a second resin layer which is formed over the first resin layer and covers a side surface of the first resin layer; and

an external terminal which is formed over the second section of the wiring pattern and is electrically connected with the wiring pattern.

23. A method of manufacturing a semiconductor device comprising:

forming a wiring pattern over a semiconductor wafer which includes an integrated circuit and an interconnect electrically connected with the integrated circuit, the wiring pattern electrically connecting with a pad which is a part of the interconnect and including a first portion located over the pad and a second section other than the first portion;

forming an external terminal on the second section of the wiring pattern;

forming a first resin layer having a side surface so that at least a part of the first resin layer is placed on the wiring pattern;

forming a second resin layer over the first resin layer so as to cover the side surface of the first resin layer; and

cutting the semiconductor wafer.